

WHAT IS CLAIMED IS:

1. A cross-connect apparatus having first to nth working cross-connects for changing over output paths of n-bit input signals that arrive from respective ones of m-number of input paths, and a connection architecture for inputting first to nth bit data of an input signal that arrives from an ith input path ( $i = 1$  to  $m$ ) to respective ones of ith input terminals of the first to nth working cross-connects and sending bit data that is output from jth output terminals ( $j = 1$  to  $m$ ) of the first to nth working cross-connects to a jth output path, said apparatus comprising:

m-number of first logic circuits respectively for calculating the exclusive-OR of the first to nth bit data of an input signal that arrives from an ith input path ( $i = 1$  to  $m$ );

a standby cross-connect having an ith terminal to which is input an output signal of a first logic circuit that corresponds to the ith input path ( $i = 1$  to  $m$ );

m-number of second logic circuits respectively for calculating the exclusive-OR of signals output from the jth terminals ( $j = 1$  to  $m$ ) of the first to nth working cross-connects and of said standby cross-connect; and

abnormality detecting means for monitoring output signals of said second logic circuits when the working and standby cross-connects have all been set to the same cross-connect state, and detecting that an abnormality has occurred in any of the n-number of working cross-connects in response to generation of an output signal that differs from that when operation is normal.

2. A cross-connect apparatus according to claim 1, further comprising:

a serial/parallel converter for converting an n-bit serial signal that arrives from each input path to a parallel signal; and

a parallel/serial converter for converting a parallel signal of n bits output from jth output terminals ( $j = 1$  to  $m$ ) of the first to nth working cross-connects to a serial signal and sending the serial signal to a jth output path.

3. A cross-connect apparatus according to claim 1, further comprising:

abnormal cross-connect specifying means which, when specifying a working cross-connect in which an abnormality has occurred, foregoes inputting signals that enter an *i*th working cross-connect to the first logic circuits, foregoes inputting signals that are output from the *i*th cross-connect to the second logic circuits, monitors whether the output signals of the second logic circuits at this time are the same as when operation is normal, increments *i* successively, thereby changing over the signals that are not input to each of the logic circuits, and decides that an abnormality has occurred in the *i*th working cross-connect when the output signals of the second logic circuits become the same as when operation is normal.

4. A cross-connect apparatus according to claim 3, further comprising:

first gate circuits for controlling gating of respective ones of the *n*-number of signals input to each of the first logic circuits; and

second gate circuits for controlling gating of respective ones of the *n*-number of signals input to each of the second logic circuits;

wherein said specifying means changes over the signals that are not input to each of the first and second logic circuits by controlling opening and closing of each of the gates.

5. A cross-connect apparatus according to claim 1, further comprising:

signal cut-off detecting means provided on an output side of each working cross-connect for detecting whether a signal from a working cross-connect has been cut off, thereby detecting an abnormality in said working cross-connect.

6. A cross-connect apparatus according to claim 1, 3 or 5, further comprising:

a controller for exercising control in such a manner that signals output from an *i*th working cross-connect will not be input to the second logic circuits when an abnormality has occurred in the *i*th working cross-connect; and

third logic circuits, responsive to a command from said controller, for replacing m-number of signals output from the ith working cross-connect with output signals of m-number of the second logic circuits.

- 5 7. A cross-connect apparatus according to claim 6, further comprising:

fourth logic circuits for checking whether output signals of m-number of the second logic circuits agree with m-number of signals output from an ith working  
10 cross-connect in which an abnormality has been detected; and

means for determining that the ith working cross-connect has returned to normal, based upon agreement of the signals that continues for a predetermined period  
15 of time.

8. A cross-connect apparatus according to claim 6, further comprising:

fourth logic circuits for checking whether output signals of m-number of the second logic circuits agree  
20 with m-number of signals output from an ith working cross-connect in which an abnormality has been detected; and

means for determining that the ith working cross-connect has returned to normal, based upon a  
25 predetermined number of successive cycles in which agreement of the signals continues for a predetermined period of time.

9. A cross-connect apparatus according to claim 1, further comprising:

30 a serial/parallel converter for converting an n-bit optical serial signal that arrives from a respective one of the input paths to an optical parallel signal;

a first optoelectronic transducer for converting  
35 said optical parallel signal to an electrical parallel signal;

a first electro-optic transducer provided on the input side of a respective one of the working cross-connects, said working cross-connects being optical  
40 cross-connects;

a second optoelectronic transducer provided on the output side of the optical cross-connect;

a second electro-optic transducer for converting  
an n-bit electrical parallel signal, which is output  
from jth output terminals ( $j = 1$  to  $m$ ) of the first to  
nth working cross-connects via the second  
5 optoelectronic transducer, to an optical parallel  
signal; and

a parallel/serial converter for converting the  
optical parallel signal output from the second electro-  
optic transducer to an optical serial signal and  
10 sending the optical serial signal to a jth output path;

wherein each of the logic circuits performs a  
logical operation based upon electrical signals.